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EXAMINER	
YU, JAE UN	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/756,861	CHARLES, ANDREW A.	
	Examiner	Art Unit	
	Jae U. Yu	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8,18,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8, 18, 21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The examiner acknowledges the applicant's submission of the amendment dated 7/3/2007. At this point claims 18, 21 and 22 have been amended. Thus, claim 8, 18, 21 and 22 are pending in the instant application.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 18 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

2. **Claims 18 and 22** are means plus function claims and interpreted according to 35 USC 112 Sixth Paragraph. However, the applicant's specification fails to disclose the corresponding means for "storing a separate busy bit map and a separate idle bit map". Thus, claims 18 and 22 are indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 21 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Garnett et al. (US 6,950,907).

2. **Independent claims 21 and 22** disclose; "creating linked lists of groups of contiguous groups **["Memory" 230, Figure 11]** of basic units **["block of main memory", Abstract]** of available user memory",

"storing a separate busy bit map **["dirty indicators", Abstract]** and a separate idle bit map **["copy of dirty indicators", Abstract]**, each bit of each map having a one-to-one correspondence with one basic unit of user memory **["each dirty indicator associated with a respective block of main memory", Abstract]**",

"wherein each active busy bit **[Element 212, Figure 11]** represents a beginning of a group of basic units **[group of "pages" 232, Figure 11]** of active user memory",

"wherein each active idle bit **[Element 222, Figure 11]** represents the beginning of a continuous group of basic units **[continuous group of "pages" 232, Figure 11]** of available user memory", and

"wherein in case portions of said user memory are inadvertently overwritten **["memory corruption" indicated by the dirty bits, Abstract]**, recreating a new set of linked lists

of available user memory **["reinstatement of an equivalent memory state in the main memory", Abstract]** from data of said busy bit map and said idle bit map".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 8 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Celi, Jr. et al. (Celi hereinafter, US 5,742,797) in view of Garnett et al. (US 6,950,907).

2. As per **independent claims 8 and 18**, Celi discloses; "assigning to each basic unit of user memory **[Memory Blocks, Figure 4A-4D]** a corresponding memory control block **[location entries corresponding to memory blocks, Figure 3]**",

"collecting groups of contiguous available control blocks into a plurality of linked lists **[linked lists of unallocated ("available") control blocks, Figure 3]**, each list for storing a plurality of elements, each element comprising a control block group having an associated minimum size user block **[The element 312 of Figure 3 indicates the size of a corresponding user memory block, wherein the list is organized according to region size from smallest available sized region ("minimum size" from the claim) to largest, Column 7, Lines 63-67]**",

"In response to a request for a block of user memory **[A request for a region of memory, Column 7, Lines 60-61]**, searching for a linked list having available control block groups corresponding to user blocks at least as large as the requested size **[Traversing the linked list to locate an unallocated** ("available" from the claim) **region of sufficient size, Column 7-8, Lines 64-6]**",

"Seizing a block of user memory of the required size **[Allocating a memory region of sufficient size for the memory request, Column 7-8, Lines 60-6]** and making available any surplus block **["Unallocated" Region 404, Figure 4A]** representing a difference between the requested size of memory **["Image #1" 402, Figure 4A]** and the size of the seized block of user memory **[Element 211D, Figure 4A]**",

"When deallocating memory **[Deallocation of a memory region, Column 8, Lines 55-54]**, testing whether user blocks of memory **[Element 402, Figure 4C]** immediately adjacent to the deallocated block **[Element 410, Figure 4C]** are available and if available merging the available blocks to the block being deallocated to create a merged deallocated block" **[After the element 402 is deallocated ("available" from the claim), it is merged with the adjacent available block (Element 410) to create a merged deallocated block (Element 412, Figure 4D)]**,

"Inserting the merged deallocated block into a linked list of available blocks of memory for containing blocks of memory of at least the size of the merged block" **[Celi Jr. et al. disclose, "Recompute the available memory region options and reform the linked list" step 604 in Figure 6, wherein the reforming includes combining contiguous unallocated regions into a single unallocated region (Column 9, Lines 39-43) and updating the linked list (Figure 3) for "Image #1" (Element 402, Figure 4C) according to the size of the merged block (Element 412, Figure 4D)]**, and

"Whereby the adding of said surplus block **[Adding the "Unallocated" Region 404 to a Linked List, Figure 3 and 4A]** and the process of creating a merged deallocated block **[Figure 4C and 4D]** helps to avoid fragmentation of memory **[Element 404 of Figure 4A and Element 412 of Figure 4D are defragmented memory blocks]**".

Celi does not disclose expressly the limitations, which are identical to those recited in claims 21 and 22.

Garnett et al. disclose the functions missing from Celi (Refer to claim 21 & 22 rejection above).

Celi and Garnett et al. are analogous art because they are from the same filed of endeavor of memory control using status bits.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Celi by including the redundant dirty indicators as taught by Garnett et al. in the Abstract.

The motivation for doing so would have been to prevent the spontaneous errors in the operation of a dirty RAM as expressly taught by Garnett et al. in column 2, at lines 20-30.

Therefore, it would have been obvious to combine Garnett et al. with Celi for the benefit of preserving system integrity to obtain the invention as specified in claims 8 and 18.

Arguments Concerning 35 USC 112 Rejections

1st Point of Argument

Regarding claims 18 and 22, the applicant states that Figure 7 discloses the "means" for storing a separate busy bit map and a separate idle bit map. However, Figure 7 merely shows the busy map and the idle bit map. Figure 7 fails to disclose what kind of an apparatus or a system ("means") stores the claimed maps. Therefore, the examiner maintains the same position regarding the 35 USC 112 rejection.

Arguments Concerning Prior Art Rejections

1st Point of Argument

Regarding independent claims 21 and 22, the applicant argues that Garnett does not show busy bit map and idle bit maps, which indicate the location and the size of

individual user memory blocks. However, the claim is silent regarding the specific location and the size of individual user memory blocks. The claim merely recites, "each active busy bit represents a beginning of a group of basic units of active user memory" and "each active idle bit represents the beginning of a continuous group of basic units of available user memory", which Garnett teaches in Figure 11 (See the corresponding claim rejection above).

Further, the applicant argues that the claimed invention is patentably distinguished from Garnett since the applicant's busy bit maps and idle bit maps can be used to reconstruct the layout of user memory. However, nowhere in the claim recites such reconstruction of memory "layout". The claim merely recites, "in case portions of said user memory are inadvertently overwritten, recreating a new set of linked lists of available user memory from data of said busy bit map and said idle bit map", which Garnett teaches in the abstract (See the corresponding claim rejection above). The examiner suggests the applicant to be more specific regarding what kind of "layout" the claimed invention actually reconstructs since the claim just discloses recreating "a new set of linked lists".

2nd Point of Argument

Regarding independent claims 8 and 18, the applicant argues that Celi and Garnett are non-analogous art. The applicant supports his argument by stating that Celi and Garnett are used for different purposes. However, both Celi and Garnett are from

the same filed of endeavor of memory access control using status indicators for storage regions. Therefore, Celi and Garnett are analogous art.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

A. Claims No Longer in the Application

Claims 1-7, 9-17 and 19-20 were cancelled.

B. Claims Rejected in the Application

Claims 8, 18, 21 and 22 have received a second action on the merits and are subject of a second action final.

C. Direction of Future Remarks

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jae Un Yu who is normally available from 9:00 A.M. to 5:30 P.M. Monday thru Friday and can be reached at the following telephone number: (571) 272-1133. If attempts to reach the above noted examiner by telephone are unsuccessful, the Examiner's supervisor, Sanjiv Shah, can be reached at the following telephone number: (571) 272-4098. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

September 13, 2007

Jae Un Yu

Art Unit 2185

J.Y.

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